REMARKS

The Advisory Action again rejects all claims under 35 USC 103.

By the above amendment, Applicant has amended the specification to clarify that it is known in the art that tautology checking generally cannot be performed with "Boolean minimization using theorems, or using Karnaugh map graphical techniques" as suggested in the Advisory Action, page 3, first paragraph. Applicant appreciates the discussion in the Office Actions on these Boolean minimization techniques.

With this clarification, it is clearer that the claimed invention has novel physical features that are not disclosed in the combination of references suggested in the Office Actions, and the novel physical features are not obvious.

1. Okuzawa's the principle of operation relies on Binary Decision Diagrams.
None of the other references cited in the rejections disclose anything related to Binary Decision Diagrams or BDDs. None of the Office Actions disclose anything related to BDDs or how to modify Okuzawa to avoid using BDDs. The claimed invention does not use BDDs, and the specification (after amendment A) points out the disadvantage of using BDDs. Therefore, the claimed invention and the modification of Okuzawa suggested in the Office Actions have **different principles**

3

of operation. "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)" according to MPEP 2143.01.

Okuzawa at Column 3, first full paragraph specifically points out BDDs' center role in its principle of operation: the two levels of logic are used to produce BDDs, and then all operations (including simplification and comparison) are based on the BDDs. Okuzawa's descriptions of FIG. 8 and FIG. 1 at Column 4 as well as its claim 1 also show the same. Therefore, by not using BDDs, the claimed invention **omits multiple key elements** (steps) in Okuzawa and it is still fully working. The other cited references do not teach how to replace these omitted elements (steps). The Office Actions do not disclose any prior art knowledge on how to replace these elements (steps) at all, either. "Note that the omission of an element and <u>retention</u> of its function is an indicia of unobviousness" according to MPEP 2144.04 (II)(B).

2. There would be no motivation to modify Okuzawa by not using BDDs. None of the cited references either explicitly or implicitly suggest avoiding BDDs in Okuzawa, and none of the Office Actions provide any motivation to avoid using BDDs in Okuzawa. According to MPEP 2143.01, "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so

4

found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." For the reasons in the next 2 paragraphs, there is no teaching, suggestion, or motivation to do so found in the knowledge generally available to one of ordinary skill in the art.

As well known in the art and as indicated in the currently amended specification, it is not practical to do equivalence checking or tautology checking with Boolean minimization using theorems, or using Karnaugh map graphical techniques. The most useful Boolean minimization theorems are about small Boolean expressions, such as A=AND(A,A). These **theorems are not likely useful on complex Boolean functions**. For example, they cannot be used to simplify well-designed multipliers in microprocessors, and therefore they do not help in showing the equivalence of 2 slightly different (but both correct) multiplier designs. It is possible to use Boolean minimization theorems about big Boolean expressions, but there can be too many of them while none of them is known as generally useful. **Karnaugh map is only useful for at most 4 or 5 variables**, and it is impractical generally because it requires explicit listing of the Boolean function's values at all points of the whole input space. Even large computer's memory can only list such values of a Boolean function with less than 50 variables. A BDD can be considered as an efficient representation of a possibly huge Karnaugh map's structure. Therefore, there is no benefit to replace BDDs with any of the conventional Boolean minimization methods.

5

Theorems and Karnaugh map techniques are taught for people to avoid simple mistakes in logic design. They are not even discussed by any references on equivalence checking or tautology checking. Specifically, the prior art discussion in Okuzawa does not include any thing related to any Boolean minimization methods. None of the Office Actions show any teaching, suggestion, or motivation to avoid using BDDs in Okuzawa.

3. There is no motivation to apply divide-and-conquer (in Tucker or any other kind) to BDDs. None of the cited references either explicitly or implicitly suggest applying divide-and-conquer to BDDs, and none of the Office Actions provide any motivation to apply divide-and-conquer to BDDs. According to MPEP 2143.01, "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." For the reasons in the next paragraph, there is no teaching, suggestion, or motivation to do so found in the knowledge generally available to one of ordinary skill in the art.

BDDs are known as very efficient representations of Boolean functions. It is generally known not good to break up BDDs in terms of subsets of the input space because it would require rebuilding the complex representations. Building one BDD may even require too much memory, and the complex process of building a BDD is

6

presented in Okuzawa at Column 6, lines 34 through Column 7, line 30 as a

recursive process doubling the number of branches for each input variable.

4. There is no motivation to apply divide-and-conquer (in Tucker or any other kind) to equivalence checking (even without BDDs). None of the cited references either explicitly or implicitly suggest applying divide-and-conquer to equivalence

checking, and none of the Office Actions provide any valid motivation to applying

divide-and-conquer to equivalence checking. According to MPEP 2143.01,

"Obviousness can only be established by combining or modifying the teachings of

the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either explicitly or implicitly in the

references themselves or in the knowledge generally available to one of ordinary

skill in the art." For the reasons in the next paragraph, there is no teaching,

suggestion, or motivation to do so found in the knowledge generally available to one

of ordinary skill in the art.

Equivalence checking compares 2 Boolean functions. Any relationship between

parts of the 2 Boolean functions does not have any implication on the equivalence

between the 2 Boolean functions. "Breaking up the Input space" as suggested in the

Advisory Action is known in the art as often not making each subproblem simpler

than the original problem. The reason is that both Boolean functions cannot be

simplified much after such breaking up. For examples, a multiplier of 31-bit data is

7

almost as big as a multiplier of 32-bit data while 4 multipliers of 31-bit data are likely much larger than 2 multipliers of 32-bit data.

5. Applying divide-and-conquer (in Tucker or any other kind) to tautology checking does not work without adding a constraint, a novel physical feature. Tautology checking with a constraint is called conditional tautology checking in the specification. There had been no known work on conditional tautology checking in any references when the application was filed. There was rarely any need of Involving such a constraint in tautology checking or in equivalence checking. When such a constraint is involved, it is the easiest to merge the constraint into the Boolean functions being checked as well know in the art, and there is no known work on any other prior art methods to use constraint in tautology check or in equivalent checking. The only reason to create the concept of conditional tautology checking is the need to apply divide-and-conquer.

The constraint represents the given subset of the input space. It is a **novel physical feature**. It is not taught in any of the cited references, and it is hardly used for anything in the art because it is usually merged into the Boolean functions defined in the subset of the input space so that the Boolean function is cleanly defined in the whole input space. Adding this novel physical feature enables applying divide-and-conquer to tautology checking. Without this novel physical feature, divide-and-conquer does not generate new and unexpected results such as getting the conclusion faster and being able to handle larger Boolean functions.

8

Because of the high cost of making the high volume VLSI chips such as the ones in computers and communication devices, it is critical to check tautology or equivalence in order to know whether the digital circuits are design correctly. Companies have put lots of money into developing methods like this. As indicated in the references, **none of them have invented this method or better methods.** If the novelty of the claimed invention were obvious to these very smart people, it would have been used widely!

6. In the remarks of Amendment B, page 6, Applicant specifically points out the supposed errors in the Final Action, paragraphs 42 and 102 (that are also in the First Action), which includes stating why they are not considered to be common knowledge or well-known in the art. No further explanation is given in the Advisory Action. **Applicant demands the examiner to produce authority for his statements** per MPEP 2144.03 (C) "If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence".

In the Advisory Action, the last full paragraph on page 2, it is asserted without any documentary evidence that "Tucker's "divide and conquer" technique may be clearly applied in breaking up the input space of a large problem into subsets of said input space, which may be processed in parallel. Tucker's "divide and conquer" problem may even simplify portions of the problem (in addition to allowing parallel

9

processing) if the subsets are selected in a rational way, for example to allow

Boolean simplifications." Remarks 3, 4 and 5 above state why they are errors under

relevant conditions and therefore not common knowledge or well-known in the art.

Applicant demands the examiner to produce authority for his statements per

MPEP 2144.03 (C).

In the Advisory Action, the first paragraph on page 3, it is asserted without any

documentary evidence that "one of ordinary skill in the art would interpret the cited

art in the view of well known Boolean input space divisional techniques such as

Boolean minimization using theorems, or using Karnaugh map graphical

techniques." These techniques are well known but not as "Boolean input space

divisional techniques" for the reasons stated in remarks 1 and 2 above. **Applicant**

demands the examiner to produce authority for his statement per MPEP

2144.03 (C).

Conclusion

For all of the above reasons, applicant submits that the specification and claims are

now in proper form, and that the claims all define patentably over the prior art.

Therefore he submits that this application is now in condition for allowance, which

action he respectfully solicits.

10

Conditional Request For Constructive Assistance

Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason, this application is not believed to be in full condition for allowance, applicant respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P. § 706.03(d) and § 707.07(j) in order that the undersigned can place this application to allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,

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11